CMOS Ultra Low-Power Wavelet Filter based Sense Amplifier for Cardiac Signal Analysis

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***Abstract*— An ultra low power CMOS implementation of an analog wavelet Gm-C filter is proposed, using MOS transistors in their strong-inversion triode region. In this region, the voltage swing can be larger than for a DTL implementation, whereas for the same dynamic range, the capacitances can be smaller, thereby saving chip area. The resulting analog wavelet filter is combined with a CMOS decision stage comprising a rectifier, a peak detector and a comparator to form a cardiac sense amplifier and the entire system is verified for QRS complex detection. Circuit simulations using UMC 130nm process validate the operation of the sense amplifier. The power consumption amounts to only 165 nW.**

I. INTRODUCTION

Cardiac signal analysis forms one of the primary functions of an implantable cardiac pacemaker. Since usually cardiac signal and noise components share the same spectral bands, discrimination of signal from noise and interference is very important. In the past few years, many new approaches to cardiac signal analysis have been proposed, such as algorithms based on filterbanks, artificial neural networks, non-linear transformations and the wavelet transform (WT). Among them, wavelet-based signal processing methods, though relatively new, demonstrate the potential for feature extraction from noisy cardiac patterns.

There are many cardiac sensing systems based on WT implemented in both analog and digital domains. The one reported in [1] by Haddad et al, uses the Dynamic Translinear (DTL) circuit technique in bipolar IC technology to implement an analog wavelet filter that implements the desired WT. Although very well suited for low-voltage, micropower applications the DTL circuit technique also suffers from some shortcomings that preclude the use in implantable devices, such as pacemakers. Firstly, as DTL circuits operate in the current domain, the input, intermediate and output signals are current-mode. Since the cardiac signal is a voltage, this necessitates a voltage-to-current converter at the input of the cardiac sensing system. Secondly, DTL circuits suffer from a limited signal-to-noise ratio (SNR), as the internal voltages are compressed. So, in order to achieve sufficient SNR, relatively large currents have to be supplied. Thirdly, the time constants realized in DTL circuits are proportional to CV_T/I_O, C being the capacitance involved in the time constant, V_T the thermal voltage kT/q, approximately 26 mV at body temperature and I_O a control current. Hence, the relatively large currents needed for a sufficient SNR also entail a large total capacitance and thus a large chip area.

In this paper, an ultra low power CMOS implementation of an analog wavelet Gm-C filter is proposed, using MOS transistors in their strong-inversion triode region. In this region, the voltage swing can be larger than for DTL, whereas for the same dynamic range, the capacitances can be smaller, thereby saving chip area. The resulting analog wavelet filter is then integrated with a CMOS decision stage comprising a rectifier, a peak detector and a comparator, and the entire system is verified for QRS complex detection.

II. QRS DETECTION

The wavelet transform is known to be a very promising tool for signal processing, particularly for local analysis of non-stationary and fast transient signals because of its good time-frequency decomposition. Due to this, WT can be utilized to extract the cardiac signal from noise. WT basically decomposes the signal into components for analysis at different resolutions (or scales). The wavelet transform of a function $f(t)$ at a scale a and position τ is given by

$$C(\tau,a)=\frac{1}{\sqrt{a}}\int f(t)\psi^{*}\left(\frac{t-\tau}{a}\right)dt \qquad (1)$$

where $\psi(t)$ is known as the wavelet base. There are many wavelet bases known, such as Morlet, Daubechies, etc, but Gaussian bases are the most often used as they provide best resolution in time and in frequency.

The algorithm for QRS complex used here is based on detection of the modulus maxima of the wavelet transform employing the first derivative of the Gaussian as mother wavelet [1]. The corresponding cardiac sense amplifier consists of a filtering stage, comprising a wavelet filter bank

with dyadic scales, followed by a decision stage, comprising a full-wave rectifier, a peak detector and decision logic. The time localization of the modulus maxima and the classification of characteristic points of the cardiac signals are processed by the digital logic circuit, and will not be discussed here.

III. CIRCUIT DESIGN

1 Filtering Stage

An analog filter has been defined, its impulse response being an approximated first derivative of the Gaussian. This particular wavelet was chosen because of its resemblance to the QRS complex and its best time-frequency resolution, a property shared among all members of the Gaussian family. A low-order transfer function was derived with the help of the Padé approximation. A 3/5 Padé approximation was chosen as it offers the minimum mean square error for a reasonable filter order, i.e., number of poles in the transfer function and number of integrating elements in the wavelet filter topology.

The transfer function thus obtained equals

$$F(s)=\frac{-0.798483+75.6128s-13.0993s^2+3.3949s^3}{43.5957+80.69s+65.7123s^2+29.9898s^3+7.88586s^4+s^5} \quad (2)$$

To decrease the complexity of the filter, an orthonormal ladder realization was chosen because it is semi-optimized for dynamic range and offers high sparsity and good behavior with respect to sensitivity. It is given by

$$A=\begin{bmatrix} 0 & 1.066 & 0 & 0 & 0 \\ -1.066 & 0 & 1.528 & 0 & 0 \\ 0 & -1.528 & 0 & 2.205 & 0 \\ 0 & 0 & -2.205 & 0 & 4.654 \\ 0 & 0 & 0 & -4.654 & -7.886 \end{bmatrix}$$

$$B=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1.584 \end{bmatrix}$$

$$C=\begin{bmatrix} 0.5322 & 2.57 & -0.8057 & 0.4605 & 0 \end{bmatrix}$$

$$D=\begin{bmatrix} 0 \end{bmatrix}$$

Gm-C integrators were used to map the above state space description onto a filter circuit topology. Since the state space description requires positive as well as negative coefficients, a differential Gm cell was used. Another advantage of using a differential cell is the cancellation of even-order distortion terms that may arise from the actual Gm implementation, thus improving linearity. As the frequency of operation is very low, it necessitates the use of either large capacitances or very small Gm's. In order to restrict the maximum integrating capacitance value to 20pF, the lowest value of Gm required is in the order of several tens of pA/V.

1) pA/V CMOS Triode-Transconductor

The Gm cell is based on the design discussed in [2]. The input stage, depicted in Fig 1, comprises a pseudo-differential input stage using PMOS transistors in strong inversion and triode (conduction) as the core Gm cell. Two current conveyors, M5,7 and M6,8, are used to relay the output currents of the pseudo-differential input stage onto the output stage and impose a well-defined drain-source voltage V_C on the input stage PMOS transistors. A scaled NMOS cascode current mirror is used with multiple outputs. Apart from the input stage PMOS transistors, all other transistors operate in weak inversion saturation. Common-gate transistors M5,6 are biased using a cascode NMOS current source. The gate voltages for M1A,2A and M1B,2B (V_{G1} and V_{G2}) are generated using a current bias generator consisting of an NMOS cascode and an external current source. The output currents of the two current conveyors are inputted into two cascode current mirror input stages and equal the transconductance factor of the above PMOSTs. This transconductance equals $Gm_1 = \beta_1 V_{tune} = (W/L)_1 \mu_p C_{ox} V_{tune}$, where V_{tune} equals the applied drain-source voltage and the other variables have their usual meaning. Control voltage V_C is generated by an identical Gm cell input stage and a servo amplifier in a negative-feedback topology. Due to the negative feedback action, V_C will be adjusted such that V_{tune} becomes equal to the externally applied tuning voltage.

The NMOS cascode current mirror output stage forms the core of the transconductor output stage that is depicted in Fig 2. Control voltage source V_{offset} is used to further reduce the Gm. Using V_{offset} also provides another parameter (besides V_{tune}) to tune the Gm of the transconductor. The upper part of the fig. depicts the common-mode output voltage negative-feedback control loop. A pair of anti-parallel diode connected thick-oxide transistors are used to generate the common-mode output voltage. This common-mode output voltage is offered to a differential pair, M5 and M6, compared with the reference voltage V_{cref} and sets the voltage at the gates of the regulated cascodes at the proper level, such that the common-mode

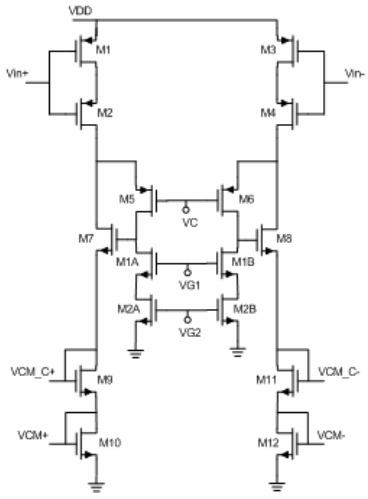

Fig. 1 Gm Input Stage

output voltage becomes equal to V_{cref}. The regulated cascode stages ensure a large (differential) transconductor output.

2) Filter Design

A fifth order differential analog wavelet filter was designed. The state space coefficients were implemented by choosing

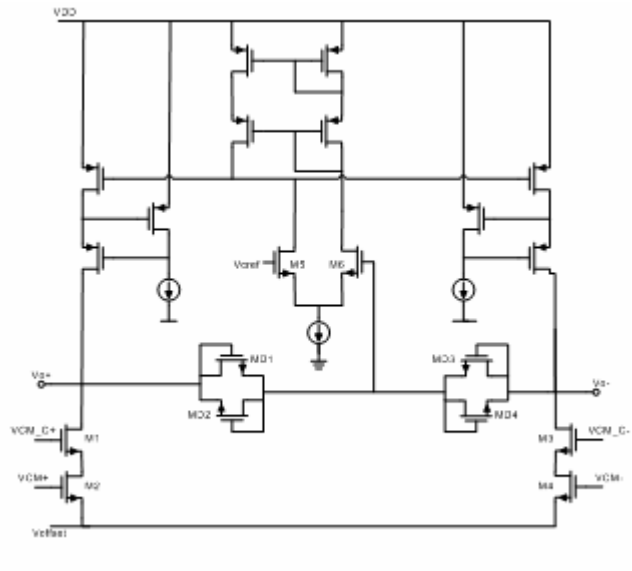

Fig.2 Gm Output Stage

appropriate widths for the NMOS cascode current mirror transistors in the output stage of the Gm cell. In order to save power and chip area, the sparsity of the *A* matrix is exploited by using only one input Gm stage per column and multiple output stages for implementing the non-zero coefficients in the *A* and *C* matrices.

2 Decision Stage

1) Full wave rectifier

The current-mode rectifier circuit is shown in Fig 3. It is based on the rectifier discussed in [3]. As all the transistors are operating in weak inversion, cascode mirrors are used to reduce the mismatch between the currents by making the drain voltages of the mirror transistors equal. Instead of using a diode-connected MOST like in [3], M1 is biased at a suitable V_{ref} in order to reduce the leakage current, and hence reduce the output current offset and power consumption. Since the input current levels can become as low as a few picoamps, the non-zero output offset current needs to be eliminated. This is performed by the combination of transistors M6,7,8,9,10, which is similar to the input stage for zero input. Voltage source V_{ref} is designed using a peaking current source and a PMOS cascode current mirror [4].

2) Peak Detector

The current-mode peak detector shown in fig. 4 is based on the concept proposed in [5]. In [5], current sources have been used to fix the biasing at the input and the output nodes. But the use of current sources introduces errors due to mismatch, which results in offset in the peak detector output. Also in [5], a diode connected transistor has been used as a switch, resulting in a significant amount of leakage.

In the circuit proposed here, a PMOST M1 is used in common-gate configuration as shown in Fig. 4. This is done to fix the voltage at the input node. Since the peak detector is used for very low frequencies, an additional capacitor is used, as the gate-to-source capacitances of M2 and M3 are not enough to hold such low voltages for a large amount of time.

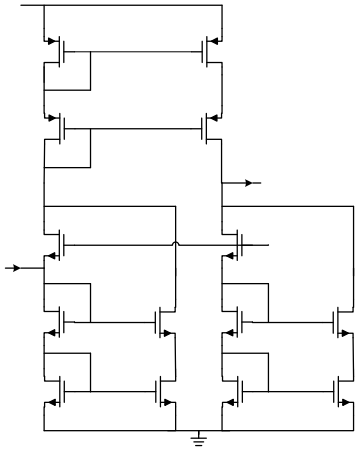

Fig. 3 Full wave Rectifier

A separate discharge path consisting of transistors M4 and M5 and current source I_{ref}, is provided. By doing so, the discharge time constant of the detector is controlled by parameter I_{ref}. A small diode D1 is connected to ensure no discharge occurs

In order to obtain a very large discharge time constant, the gate voltages of the transistors M4 and M5 are cross-coupled to obtain a discharge current of the order of few femtoamps. A regulated cascode is used to increase the resistance at the peak detector input node, in order to make the peak detector more sensitive. The biasing currents I_{bias} for the regulated cascode structures are obtained by copying the PMOS cascode current mirror outputs of the rectifier.

By subtracting the peak detector output from the 4/3 times the rectifier output, a bipolar current is obtained that is positive only when a peak occurs [6]. This current is offered to the final block in the system, the current comparator.

3) Comparator

A current switching CMOS current comparator [7] is used. Its operation is as follows: for positive input currents, the voltage at the input node increases. This results in the CMOS inverter driving Mp into its ON state. Similarly, for negative input currents, Mn is driven into its ON state. The feedback loop around the inverter and Mp & Mn also helps in limiting voltage excursions at the input node. Another inverter is used

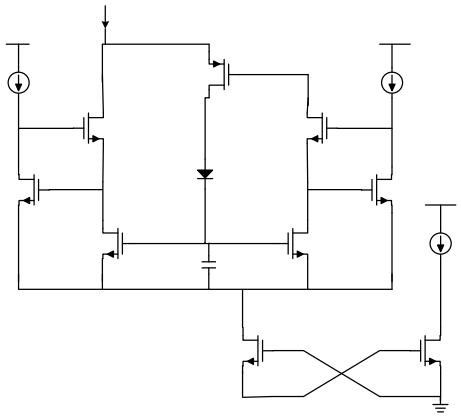

Fig. 4 Peak detector

as a binary buffer, to restore the desired output voltage levels and to drive the load (here modeled as a load capacitance C_L). To reduce leakage, thick-oxide transistors are used possessing a high threshold voltage.

IV. Simulation Results

The operation of the sense amplifier was verified using circuit simulations in UMC 130nm CMOS IC technology. Typical process characteristics are: multiple threshold voltages (NMOS/PMOS: 0.38/-0.33; 0.47/-0.42; 0.58/-0.52), twin well, thick gate-oxide option, 8 metal layers, 110GHz maximum transit frequency. The system has been designed to operate from a 1.2V supply voltage.

From circuit simulations, it was observed that the AC response of the wavelet filter exactly follows the AC response of the filter as plotted from the intended transfer function. Fig. 6 shows the impulse response of the wavelet filter, which indeed approximates the Gaussian monocycle (gauss1) very well. Wavelet filter tuning voltage V_C was chosen to be 10mV (referred to V_{DD}). I_{bias} and V_{offset} were chosen to be 5nA and 45mV, respectively. For implementing other (dyadic) wavelet scales, the desired passbands and time constants can be selected by modifying the V_{offset} or V_{tune} or by scaling the widths of the output current mirror transistors accordingly.

Fig. 7 shows the DC responses of the full wave rectifier and the comparator, with V_{ref} set at 150mV. The transient response of the peak detector, with I_{ref} equal to 5nA for a periodic pulse train as input is shown in Fig. 8. Finally, Fig. 9 shows the transient responses of the entire system. The power consumption of the entire system amounts to 165nW per scale.

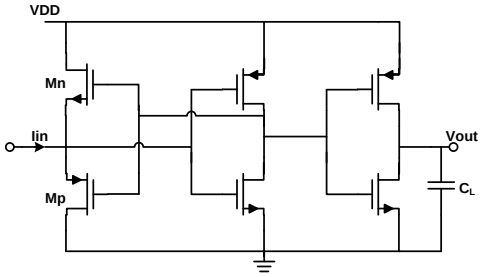

Fig. 5 Comparator Circuit

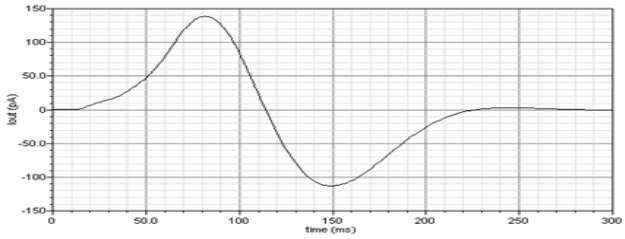

Fig. 6 Wavelet Filter (gauss1) Impulse Response

V. Conclusion

An ultra low power CMOS implementation of an analog wavelet Gm-C filter has been proposed, using MOS transistors in their strong-inversion triode region. The analog wavelet filter is combined with a CMOS decision stage comprising a rectifier, a peak detector and a comparator to form a cardiac sense amplifier and the entire system is verified for QRS complex detection. The whole system is highly programmable and operates from a 1.2V supply voltage, consuming 165nW. The obtained results for a typical cardiac signal demonstrate a good accuracy in generating the desired Wavelet Transform and achieving correct QRS complex detection.

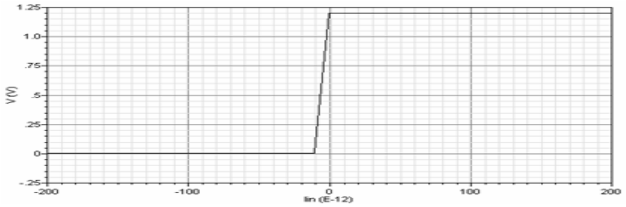

Fig. 7 DC response of the full-wave rectifier (above) and of the comparator (below)

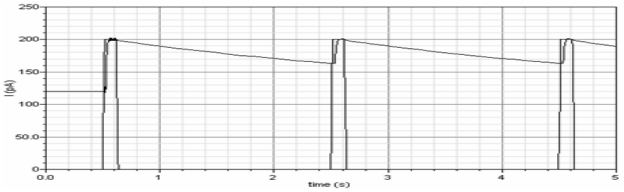

Fig. 8 Transient response of the peak detector

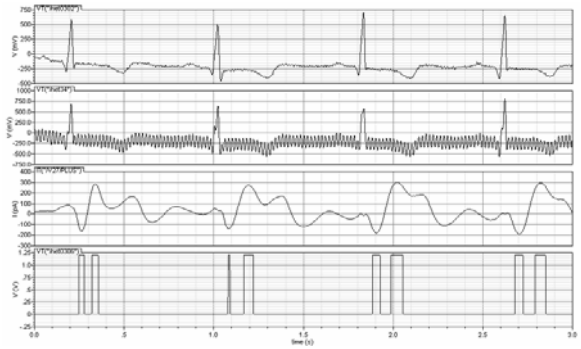

Fig. 9 Transient responses of the wavelet filter (3rd line) and the comparator for a stylistic cardiac signal (1st line) contaminated with 50Hz interference (2nd line)

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