Matched FET Cascode Pair: Design of Non-Linear Circuits without DC Biasing Supply

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***Abstract* - In this brief, a novel low voltage basic cell, coined as the Matched FET Cascode Pair, has been proposed. The approach exploits the non-linear characteristics of transistors in the triode region. The cell requires complimentary input signals, with the gate voltages of the FETs acting as the control signals. Several non-linear circuits designed without the help of DC biasing, are described and a set of measured and simulation results of both - the JFET and MOSFET implementations, are shown to demonstrate the design flexibility of the approach.**

***Index Terms*-Analog Circuits, Circuit Topology, FET Circuits, Nonlinear Circuits**

I. INTRODUCTION

During the last few years, designers have strived for circuit architectures which employ reduced power supply voltages. This trend has been supported by device downscaling, which implies a reduction of the chip area and thus results in higher packing density in integrated circuits. The reduction of power supply voltage offers an additional advantage, decrease of power consumption in integrated circuits. This is an important issue not only in battery-operated circuits, but also in very large-scale integrated circuits, where heat dissipation is not a negligible factor anymore.

Circuit operation at reduced voltages is a common practice adopted to reduce power consumption. However, at low voltages, the circuit performance degrades along with bandwidth and voltage swings. This generates a need for adoption of alternative design techniques to suit the low voltage environments. All these factors have spurred on a new direction in analog design, namely low voltage circuit design [1].

Several circuit techniques and architectures have been proposed to reduce the supply voltage requirements in analog and mixed-signal circuits, among them: folding, subthreshold operation of mosfets, bulk-driven, level shifters, floating gate techniques, flipped voltage followers and current mode processing. The use of these techniques along with aggressive scaling, have led to the reduction of supply voltages to 0.5V [2].

The holy grail of low voltage analog circuit design is to realize circuits which can/could operate without any DC biasing supply. Such circuits should be able to derive their biasing requirements solely from the input supply. A few such circuits have been introduced by Ciubotaru [3-8]. Building upon these foundations, the authors take a significant step towards the design of such circuits, by introducing the Matched FET Cascode pair. The FET cascode pair is a novel two-transistor block, designed for operation with sub-1V input voltage signals. It has been employed to design several non-linear circuits without using DC Biasing supply, as discussed in the next few sections of the brief.

II. DESIGN CONSIDERATIONS

There are several difficulties that restrict the design and application of circuits without DC biasing in VLSI circuit design. Such circuits, apart from being very difficult to design, face serious performance issues. Firstly, there is no amplification possible, as the only power provided to the circuit originates from the input signal itself. Also the dynamic range of the circuit is limited by the input voltage swing.

As the biasing for all the transistors is derived from the input voltage, a large input swing might change the region of operation of a particular transistor, altering the behavior of the entire circuit. This restricts the input signal range, thereby reducing the domain of non-linear circuits which can be effectively realized by such circuits.

III. MATCHED FET CASCODE PAIR

The proposed analog cell is shown in fig. 1. It consists of a matched pair of symmetrical n-channel JFETs connected in a cascode. V_{in} is kept small, so that the transistors work in triode region. Applying the current equations-

$$I_{D1} = I_{DSS}\left[2\left(1-\left(\frac{V_A - V_{out}}{V_P}\right)\right)\left(\frac{V_{in}-V_{out}}{-V_P}\right)-\left(\frac{V_{in}-V_{out}}{V_P}\right)^2\right]$$

$$I_{D1} = I_{DSS}\left[2\left(1-\left(\frac{V_{in}+V_B}{V_P}\right)\right)\left(\frac{V_{out}+V_{in}}{-V_P}\right)-\left(\frac{V_{out}+V_{in}}{V_P}\right)^2\right]$$

Now, $I_{out} = I_{D1} - I_{D2}$

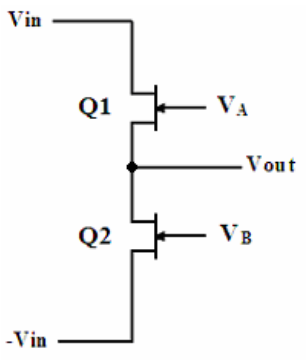

Fig. 1 Matched FET Cascode Pair Topology

$$= k\left[2V_{out}V_P - (V_A + V_B)V_{out} + (V_A - V_B)V_{in} - V_{in}^{\,2}\right] \quad (1)$$

where $k = \dfrac{I_{DSS}}{2V_P^2}$

In the above circuit, V_A and V_B are referred to as control inputs. By manipulating the values at these inputs, several non-linear circuits have been designed.

The square-law circuit [3] can be easily deduced from the matched cascode JFET pair, by making $V_A = -V_B = V_{in}$ in eqn. (1). Assuming $I_{out} \approx 0$,

$$V_{out}^2 + V_{in}^2 + 2V_{out}V_P = 0 \quad (2)$$

Since V_{out} is appreciably < V_{in} in this configuration, $V_{out}^2 << V_{in}^2$ is a reasonable approximation, which leads to the following simplification –

$$V_{out} \approx \frac{V_{in}^2}{-2V_P} \quad (3)$$

Similarly, by putting $V_A = V_B = V_{OUT}$, an inverting square-law can be obtained [5], having output as –

$$V_{out} \approx \frac{V_{in}^2}{2V_P} \quad (4)$$

By making $V_A = V_B = V_P$, another important function can be derived from this structure – absolute-value circuit [4], shown in fig. 2.

On replacing these values in (2),

$2V_{out}^2 + V_{in}^2 = 0$

or $V_{out} = -1/\sqrt{2}\,|V_{in}|$ (5)

IV. MATCHED FET CASCODE PAIR

Despite the similarity between JFETs and MOSFETs, the same topology when implemented in n-channel depletion type MOSFETs, gives a much poorer performance due to the body effect.

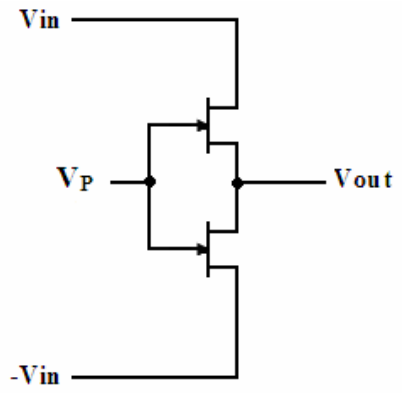

Fig. 2 Absolute Value Circuit [4]

It is known that for a p-n junction to be effectively forward biased, the bias voltage across the junction should exceed a particular value, called the cut-in voltage. This is because the current is negligibly small for voltage smaller than cut in voltage, 0.5V in case of Si, owing to the exponential relationship between voltage and current [9]. Exploiting this effect, the cascode pair using MOSFET can be made to work by simply grounding the body terminals, provided the input swing is limited to ±0.5V.

Though the above configuration is simple and easy to implement, its performance is quite error-prone and the input swing has been effectively halved. Two more blocks are discussed below, which use extra circuitry to resolve these issues.

The first MOSFET implementation is shown in fig 3. The body connection is switched through using something similar to pass-transistor logic. In the circuit shown, all transistors used are n-channel depletion MOSFETs, with M1 and M2 having V_{TH} = -1 and M3, M4, M5 and M6 having zero threshold voltage. As V_{in} switches from positive to negative, the drain and source terminals of M1 and M2 interchange. M3, M4, M5 and M6 being zero threshold devices, go into cutoff and triode regions accordingly, resulting in substrate remaining in contact with the source terminal throughout the input swing.

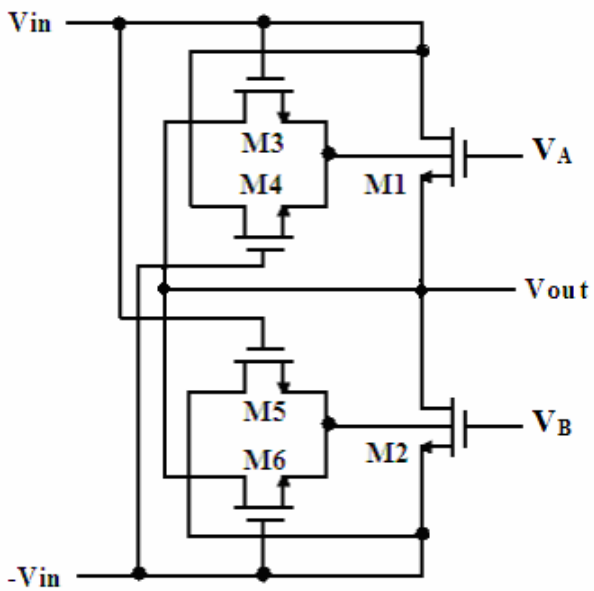

Fig. 3 MOSFET Implementation of Cascode Pair (1)

Zero-threshold devices can be fabricated by adding an extra masking and ion-implantation step to the basic NMOS process, so that even at V_G = 0, a channel between the source and the drain exists. In this case, to deplete the channel, negative voltage has to be applied. MOSFETs with zero-threshold voltage can also be obtained by using two-input FGMOS transistors [10].

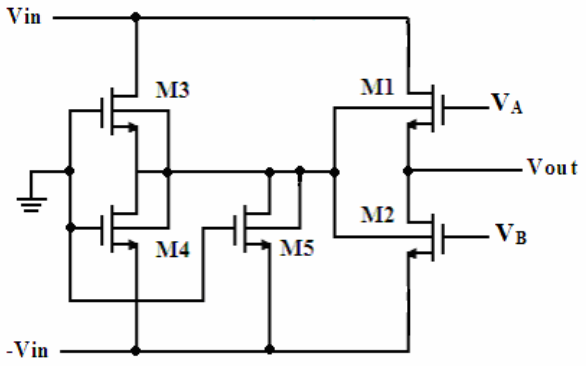

Fig. 4 MOSFET Implementation of Cascode Pair (2)

Another implementation can be derived from the fact that for most circuits comprising of n-channel MOSFETs, the body terminals are connected to the most negative supply available in the circuit. This ensures that the source-body junction remains in reverse biased condition through out the operation of the MOSFET. However, this cannot be accomplished in the proposed cell as V_{in} ranges from -1 to +1 V.

To overcome this problem, an inverting modulus circuit, described in the previous section, is used to generate -|Vin|, which acts as the most negative point and is, thus, used to bias the substrate terminals of all the MOSFETs. As shown in fig. 4, the lower MOSFET is replaced by two identical MOSFETs connected in parallel, so as to obtain a unity transfer ratio. Any external voltage supply can be avoided by using zero-threshold devices.

V. DESIGN OF NONLINEAR CIRCUITS

The FET Cascode pair can be used as a fundamental building block in analog circuit design. Several non-linear functions have been realized by Ciubotaru in [3-8], such as squarer, cuber, four-quadrant multiplier, etc. It can be seen that all these circuits are based on the proposed FET cascode pair. In this section, circuits realizing a few more common non-linear functions are discussed –

(a) Mean Square Circuit

A two-input mean square circuit, shown in fig. 5, has been designed by employing two matched FET cascode pairs, Q1-Q2 and Q3-Q4. It can be shown that both the pairs are operating as squarers.

As shown in fig. 5 -

$$I_{d1} + I_{d3} = I_{d2} + I_{d4} \qquad (6)$$

On putting their respective expressions and simplifying, the output voltage is obtained as –

$$4V_{out}V_P = 2V_{out}^2 + (V_{in1}^2 + V_{in2}^2) \qquad (7)$$

If $V_{in1}^2 + V_{in2}^2 >> 2V_{out}^2$, then –

$$V_{out} = \frac{V_{in1}^2 + V_{in2}^2}{-4V_P} \qquad (8)$$

For an N-input mean square circuit, (8) can be generalized as -

$$V_{out} = \frac{\Sigma V_{in}^2}{2NV_P} \qquad (9)$$

It may be noted that as the number of inputs increase, the approximation made becomes less reliable and the error increases.

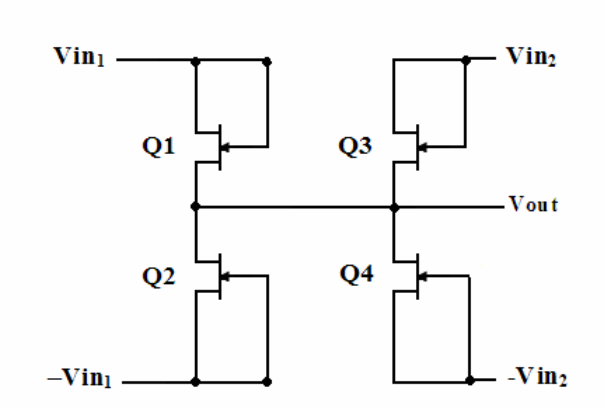

Fig. 5 Mean Square Circuit

(b) Difference-of-Squares Circuit–

A difference-of-squares circuit basically computes the difference between the square of two voltage signals. It can be used for various applications, like R.M.S.-to-D.C. conversion [11], etc. The circuit, shown in fig. 6, uses two JFET squarers of opposite polarity.

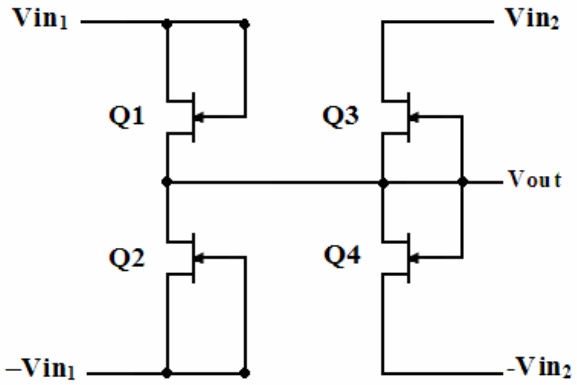

Fig. 6 Difference of Squares Circuit

It can be seen that,

$$V_{out} \approx (V_{in1}^2 - V_{in2}^2)/4V_P \qquad (10)$$

$$\approx (V_{in1} + V_{in2})(V_{in1} - V_{in2})/4V_P \qquad (11)$$

If $V_{in1} = V_c + Vd$ and $V_{in2} = V_c - V_d$, then

$$V_{out} = V_c V_d / V_P \qquad (12)$$

where V_c = Common voltage = $(V_{in1} + V_{in2})/2$

V_d = Differential voltage = $(V_{in1} - V_{in2})/2$

(c) Voltage Controlled Resistor

Fig. 7 shows a voltage controllable resistor, constructed

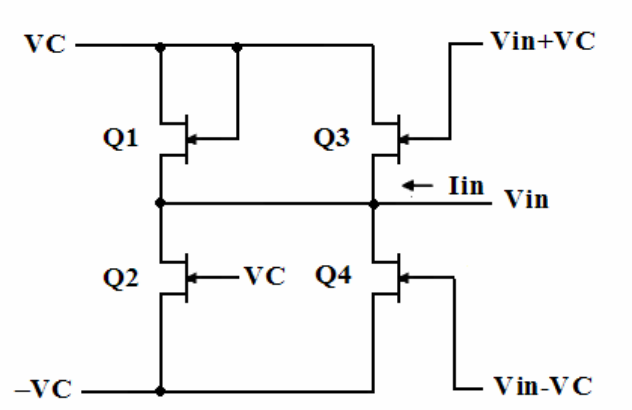

Fig. 7 Linear Resistor

using two matched JFET cascode pairs, Q1-Q2 and Q3-Q4. For pair Q1-Q2, the control inputs are –

$V_A = V_B = V_C$

and for Q3-Q4, the control inputs are –

$V_A = V_{in} + V_C$; $V_B = V_{in} - V_C$

Following a similar procedure for analysis, the current I_{in} is obtained as –

$$I_{in} = 2KV_{in}(V_C - 2V_P) \quad (13)$$

and $$R_{in} = V_{in}/I_{in} = 1/[2K(V_C - 2V_P)] \quad (14)$$

The equation (13) shows that the input voltage, V_{in} and input current, I_{in} have a linear relationship and the equivalent input resistance is dependent on V_C, the control voltage and V_P, the pinch off voltage of the transistors. Hence, it can be used as a voltage controllable one-port active resistor.

VI. FUNCTION GENERATION USING MACLAURIN'S SERIES

In [3,5-6], square-law, cube-law and 4th-power law have been realized using the cascode pair. Using a combination of these circuits, circuits realizing other functions can also be designed with the help of Maclaurin Series.

The Maclaurin series expansion for exponential circuits is given as [11]–

$$e^x = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} + \ldots \quad for -\infty < x < \infty \quad (15)$$

The exponential law can be suitably implemented with the transfer function as –

$$V_{out} = k_1 V_{TH}\left(e^{k_2 V_{in}/V_{TH}} - 1\right) \quad (16)$$

where k_1 and k_2 are constants.

Using Maclaurin series expansion, the above equation can be written as –

$$V_{out} = k_1 V_{TH}\left[\left(\frac{k_2 V_{in}}{V_{TH}}\right) + \frac{1}{2}\left(\frac{k_2 V_{in}}{V_{TH}}\right)^2 + \frac{1}{6}\left(\frac{k_2 V_{in}}{V_{TH}}\right)^3 + \ldots\right] \quad (17)$$

$$\text{Or } V_{out} = k_1\left[\left(k_2 V_{in}\right) + \frac{1}{2}\frac{\left(k_2 V_{in}\right)^2}{V_{TH}} + \frac{1}{6}\frac{\left(k_2 V_{in}\right)^3}{V_{TH}^2} + \ldots\right] \quad (18)$$

Since V_{in} is less than 1, a reasonably accurate value for V_{out} can be obtained by considering only the first four terms, that is, till n=3. For k_1=k_2=1, V_{in}=V_T and considering the first few series terms, an error of only 1.89% is obtained.

Equation (18) may be obtained by combining the square-law and cube-law blocks along with the input voltage. In fact, if V_T can be provided in the circuit, a purely exponential relationship between input-output voltages can be obtained!

Similarly, other functions such as hyperbolic, sinusoidal, etc can be realized by combining the square law and cube law outputs. A possible way of summing these blocks is to use a multiple-input floating gate MOSFET. All the voltages provided to the multiple gates of the MOSFET, are capacitively coupled in ratios proportional to the dimensions of the multiple gates. The summed output can be obtained by using a differential amplifier.

VII. RESULTS

The JFET circuits described in the previous sections were verified by using BF245C n-channel JFETs. The measured parameters of the JFETs were IDSS = 12mA and VP =-2V. The DC characteristics were measured and verified using a load RL = 10KΩ.

The MOSFET implementation of the previously discussed circuits was verified with the help of PSPICE simulations carried out on 1.5 µm CMOS technology. The DC transfer characteristics for some of the circuits have been given below.

VIII. CONCLUSION

A novel two-transistor analog cell, Matched FET Cascode Pair, has been proposed for low voltage operation. Using this

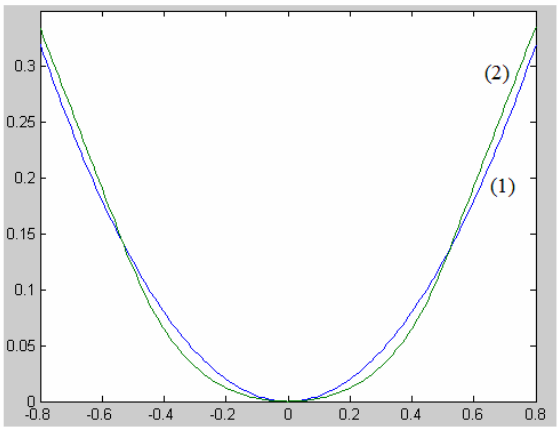

Fig. 8 MOSFET Squarer (1) Ideal Response (2) Circuit Response

cell as the basic building block, a number of non-linear analog circuits have been designed, which are essentially voltage-mode in nature and work well for sub-1 volt range. These circuits have a significant advantage in that they do not require any DC biasing supply; the biasing for all the FETs used being derived from the input signal voltage itself.

Using the nth power circuits based on the analog cell, a number of functions frequently used in analog computing can be generated through Maclaurin's series expansion.

The JFET and MOSFET Implementations of proposed circuits have been verified using BF245C n-channel JFETs and through PSPICE simulations on 1.5μm CMOS technology, respectively.

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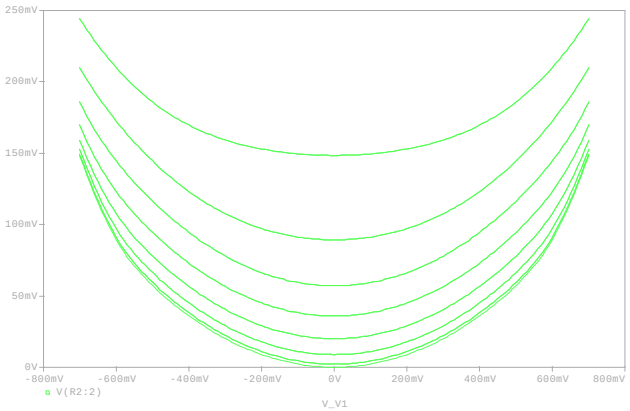

Fig. 9 MOSFET Mean Square Circuit

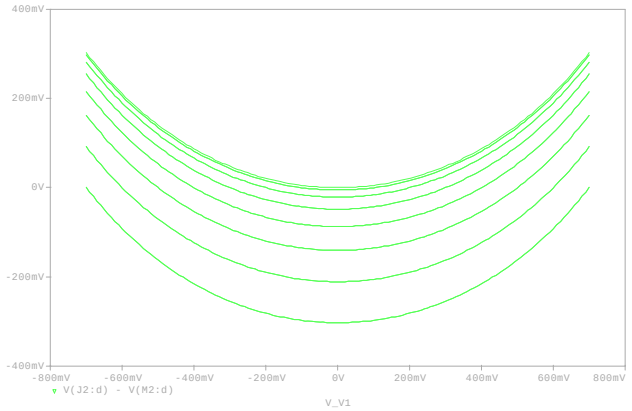

Fig. 10 MOSFET Difference of Squares Circuit

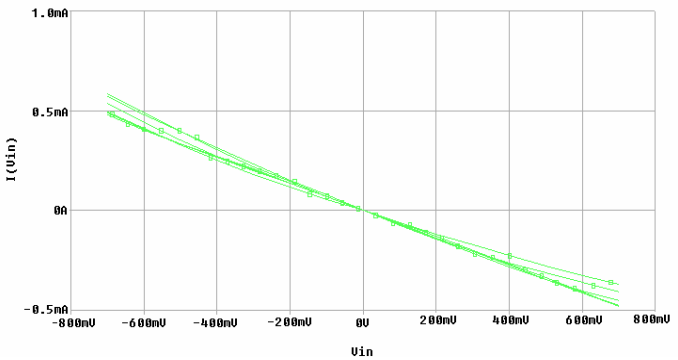

Fig. 11 MOSFET Linear Resistor

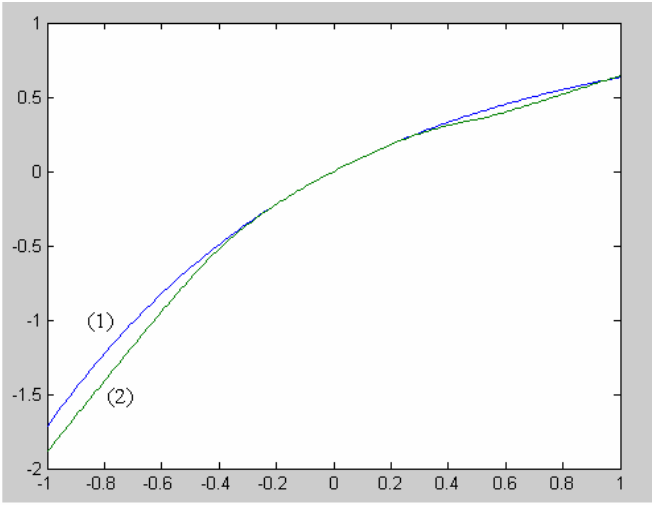

Fig. 12 MOSFET Exponential Law Circuit (1) Ideal Response (2) Circuit Response